

In-chip Monitoring for Extended Reliability Testing and Mission Profile Monitoring Feedback Loop

Andrea Matteucci, *Product Manager*

proteanTecs, 36 Kdoshei Bagdad St., Haifa 33032, Israel; Andrea.Matteucci@proteanTecs.com

Luca Moriconi, *R&D Manager*

ELES, Todi – PG – Italy; luca.moriconi@eles.com

Abstract—The reliability challenges of modern automotive and mission critical applications poses the risk that classical way of reliability testing, such as those outlined in industry standards like JEDEC JESD47 and JESD22, is insufficient. The mission profile at the base of existing standards were established decades ago and might not be representative of the requirements of modern mission-critical SoC, particularly those based on advanced FinFET nodes slated for deployment in the next generation of vehicles. To address this gap, innovative approaches are needed to guarantee the application of the adequate stress vs. mission profile, to measure performance degradation more precisely, and with fine granularity, simplifying the search for root cause analysis (RCA) and enabling an effective design for Zero Defects. This paper will explore the integration of advanced reliability test equipment, such as ELES ART5xx in combination with proteanTecs in-chip digital monitoring IP and analytics. Leveraging deep data extracted from in-chip monitors enables running more complex test sequences and checking their response on board during the oven stress time. The outcome is an efficient stress test capable of identifying and addressing design and process vulnerabilities.

Keywords—Semiconductor, Advanced Analytics, Test, Reliability, JEDEC, HTOL, Burn-In, Degradation Monitoring, On-Chip Monitoring, Design for Reliability Test, Test for Reliability

I. INTRODUCTION

Reliability testing are designed considering that subjecting a device to operate under elevated temperature and voltage mirrors the stress it would encounter throughout its intended lifespan. This is achieved by applying an Acceleration Factor (AF) derived from the Arrhenius equation. The conventional JEDEC [1] HTOL test involves a minimum group of randomly selected 77 units of three lots. At predefined intervals (0, 48, 168, 500, 1000 hours), the devices undergo the complete Final Test (FT) patterns. A test is considered as pass if, after the last verification, none of the devices experienced a failure. However, even a single failed device means the repetition of the entire test flow.

There are critical aspects of this Reliability Testing Procedure:

- The usage on a randomly selected group of devices introduces the risk of including outlier devices with latent defects or manufactured outside the allowed

process window. A failure of such outlier device invalidates the entire test, leading to significant financial and time investments being wasted.

- Stress recovery effects can affect off-oven measurements, compromising the accuracy of performance degradation evaluation. Stress and testing procedures must be concurrent for reliable results.
- With the shift towards electrification and assisted driving in automobiles, the industry faces the need to address extended (long-duration) mission profiles beyond the traditional 1000-hour HTOL test duration [2]. Failure to account for longer mission profiles may lead to an incomplete understanding of the device's reliability in real-world automotive applications.
- A binary pass/fail assessment lacks quantitative data on degradation and remaining margin-to-fail. Inability to measure the degradation and margin-to-fail hinders the understanding of the device's health and reliability.
- The test environment itself can contribute to failures due to issues such as incorrect temperature and voltage settings, defective components on the board, such as sockets, or inappropriate stress patterns. This potential risk of reduced confidence highlights the importance of environmental control and the ability to measure the impact on the devices during the test execution.

The paper describe the benefits of integrating proteanTecs Performance and Health Monitoring (PHM) system with ELES ART reliability test platform and Test for Reliability (TfR) methodology. Through in-chip monitoring, early failure detection, and mission profile validation, the integration offers valuable data to mitigate inaccuracies and errors induced by inaccurate test conditions, stress recovery effects, machinery faults, or outliers. This holistic approach results in an overall reduction in costs and enhanced confidence in the testing process.

II. PROTEANTECS IN-CHIP MONITORING

proteanTecs Performance and Health in-chip monitoring solution is comprised of monitoring IPs, called Agents, that are designed into the IC and measure vital performance indicators during test or in normal operation mode, such as voltage noise, local internal temperature, clock jitter, and timing performances. proteanTecs data analytics software is deployed at the Cloud or on the Edge (e.g., on the Automated Test Equipment) to analyze real-time the data and provide insights about how the IC is performing during its operation.

III. ELES ART5XX PLATFORM

The ELES ART5xx [3] adaptive reliability test platform allows to combine the application of accelerated stress and test together in the same equipment during qualification trials, leveraging IC specifically designed for reliability tests and testability (DfRT).

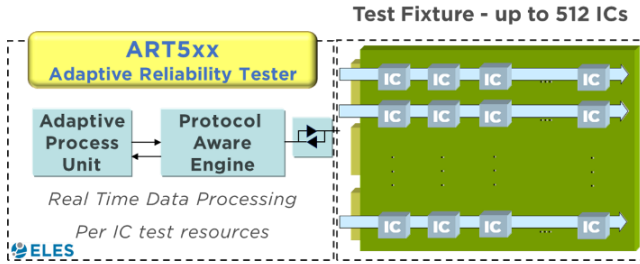


Figure 1: ART: DfRT Adaptive Tester

The continuous assessment of device performance and degradation under stress conditions is concurrently recorded throughout the entire qualification lots. To augment reliability measurements, the embedded in-chip measurement feedback from proteanTecs Agents is seamlessly integrated into the test flow.

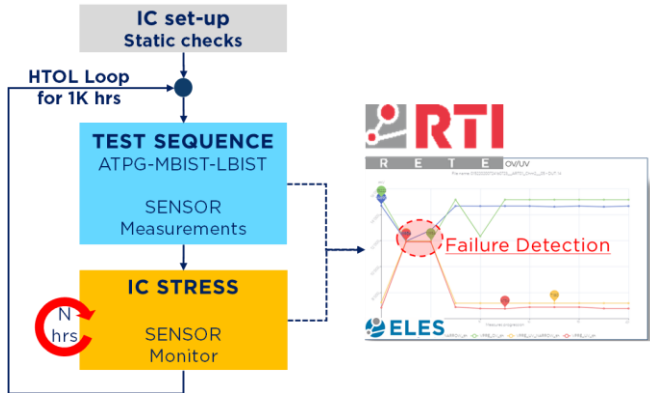


Figure 2: TjR – HTOL Test & Stress in the same flow

The main benefits of test flow enriched by Agent measurements are:

- Full and real time control of applied stress in combination with parallel range of digital monitors for voltage, temperature, and toggle rate;

- Possibility to apply adaptive stress/test strategies based on measurement feedback;
- Continuous non intrusive performance measurements with fine granularity going beyond standard checkpoints on ATE;
- Avoiding stress recovery effects due to separate stress and test phases;
- Qualification experiment automatization, eliminating the need to move parts between different equipment, saving weeks compared to the standard process.

IV. SMART MATERIAL SELECTION

The standard operating procedure for selecting devices to be HTOL tested according to JEDEC, calls for random selection of devices from 3 consecutive lots. In practice, they are selected from different corner lots with the assumption that this will provide full coverage for the process manufacturing range. This is no longer sufficient as the parametric variation is too wide in advanced process nodes.

We propose a new method of selecting the samples that will represent the widest parametric variation from each of these lots. It is based on proteanTecs Classification and Profiling Agents that map each area in the chip to its representative manufacturing parameters based on the simulated Process Design Kit (PDK). This creates a high resolution “Die Fingerprint” for each area in each die on the wafer, as can be seen in Figure 3 below, and algorithms running on the cloud to find those with the widest parametric distribution.



Figure 3: Die fingerprinting using ML-driven deep data

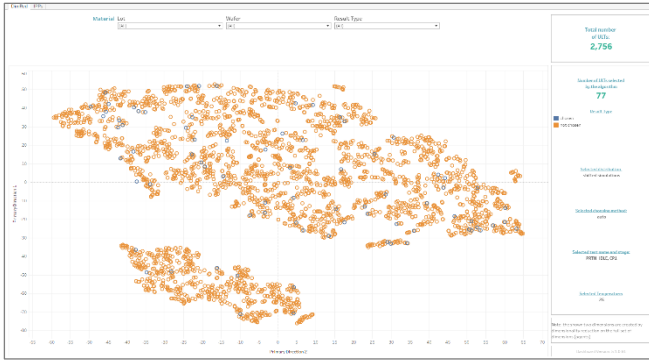


Figure 4: Smart Material Selection in the cloud

In Figure 4, we see an example of selection of 77 units (marked in blue) out of available 2,757 (orange) from one lot, that were chosen to provide the widest parametric coverage of the PDK.

V. DEGRADATION MONITORING AND OUTLIER DETECTION

While in the oven and running structural or functional test patterns, proteanTecs Classification and Profiling Agents will continue to monitor the parametric variation (e.g. leak current) of each of the transistor types and representative cells used in the design.

This can be seen in the following image, Figure 5.

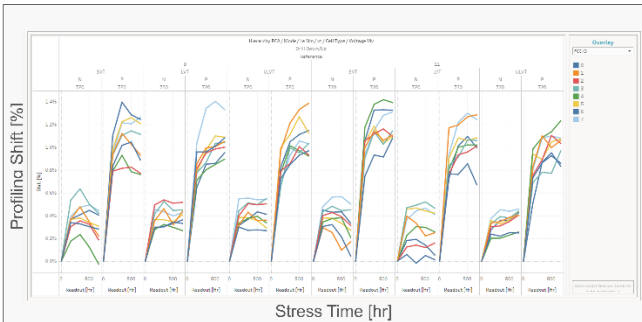


Figure 5: Degradation per transistor type

In addition, proteanTecs Performance and Degradation Monitoring Agents are used to measure the change in performance over time and compare the degradation between batches. They continuously track the remaining timing to the target clock frequency at very high coverage (billion of logical paths): by analyzing these trends over time, we can visualize the degradation effects in each small section of the design and predict time to failure.

In Figure 6, the degradation of actual logic is illustrated by plotting the remaining timing margins to the target clock. Notably, a specific logic area in the design, the points shown in purple, is exhibiting a faster degradation compared to others. This suggests a potential risk if failure before the 500 hours mark. If this degradation pattern would be observed across all samples, it could signal an overstressed region in the chip, or a design sensitivity. However, only one unit displays

such a behavior, and it may indicate a latent defect. In such cases, it is preferable to halt the test and restart with a fresh set of units, rather than investing more time only to encounter a functional test failure later on.

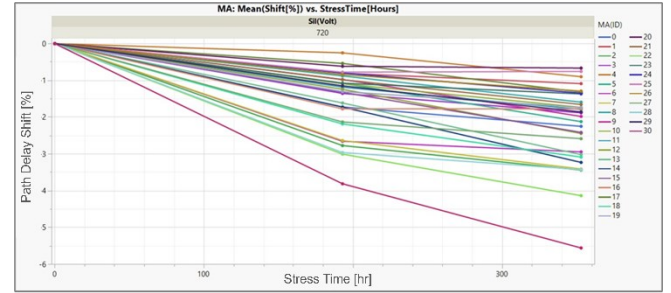


Figure 6: Timing degradation monitoring

For holistic real-time, continuous monitoring of the degradation of each Device Under Test (DUT) while in the ELES ART reliability test platform, proteanTecs edge software application visualizes the temperature, voltage, stress, and worst timing margin over time. It calculates the reliability distribution and time-to-failure prediction as shown in Figure 7.

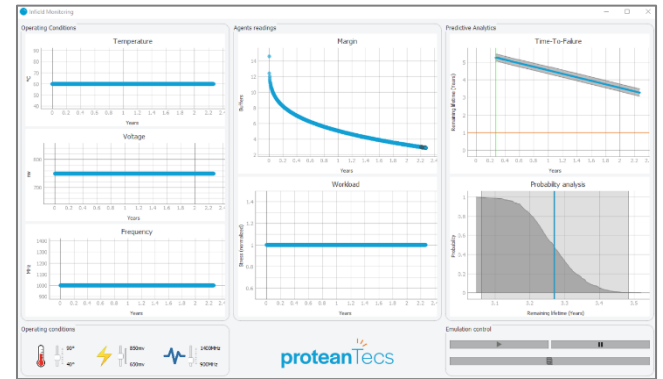


Figure 7: Real time degradation monitoring

VI. MISSION PROFILE VALIDATION

Automotive semiconductors are designed with Mission Profile in mind, which refers to a description of the qualifying stress system or its component parts are expected to experience during life. The stress for semiconductors is characterized by a combination of voltage, temperature, and activity rate for a certain percentage of the device lifetime. proteanTecs Workload Agents are designed to continuously and concurrently measure the stress combination of the three contributors. Figure 8 shows how the specifications for Mission Profile are converted to the expected reading of the different Workload Agents.

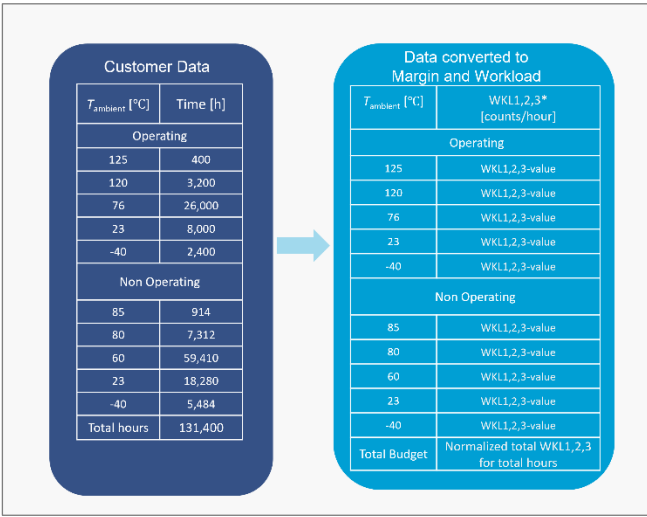


Figure 8: Mission Profile data conversion to Workloads (arb. units).

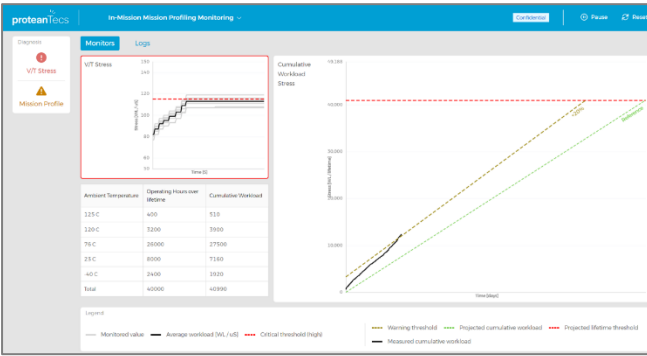


Figure 9: Mission profile validation

In Figure 9, we demonstrate an application running on the HTOL tester to monitor the Mission Profile budget consumption during the stress test. The stress measured during the HTOL test is monitored via the Workload Agents during the test to validate if it is equivalent to the specifications. In addition, the application will display in real time, to predict remaining time to consume the Mission Profile budget.

ELES ART platform, thanks to its adaptive stress and test capabilities can read Workload Agents feedback from the software at the edge and adjust in real time the relevant stress matrix in order to better match Mission Profile and trial duration targets.

VII. BURN-IN WITH CONFIDENCE, ENVIRONMENT VALIDATION AND RCA

An underlying assumption for the reliability of the HTOL test is a correct and uniform setting of voltages and temperatures in the oven. This is typically achieved by using sensors on the load board. The example below (Figure 10), shows an early alert of a non-uniform degradation that was observed, and had triggered a root cause analysis with the customer. In this example, two boards are shown, BIB 2 and BIB 10. BIB 2 shows a normal distribution of the degradation

as the higher degraders (red) are randomly distributed. On the other hand, BIB 10 shows a very distinctive pattern that that “lower” half is degrading more than the “upper” half.

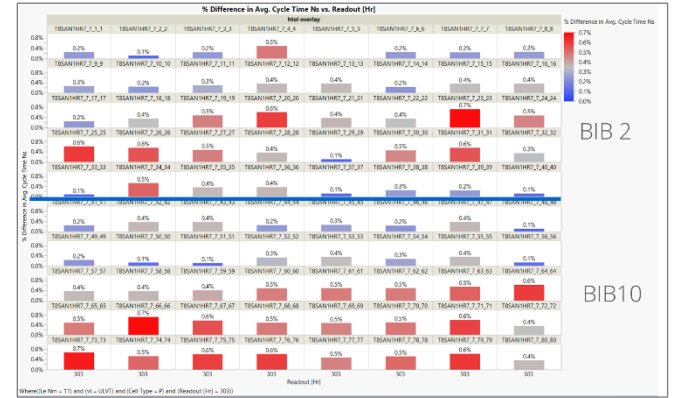


Figure 10: Degradation anomaly detection

The proteanTecs Local Voltage and Temperature Sensors were used to extract accurate measurements from within the DUTs, for improved accuracy and higher distribution. The Data Analytics Platform was used to generate a spatial image out of these readings for easy and early identification of wrong voltage or temperature settings, or unintended gradient across the DUTs. Such a visualization is shown in Figure 11 below, showing correlation of lower-than-expected degradation, to lower temperature on the “upper” half of the board.

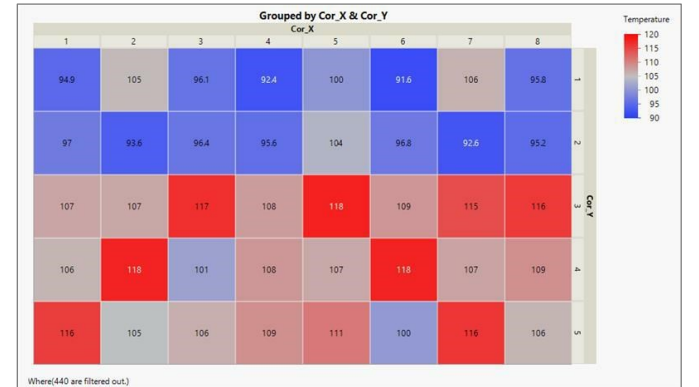


Figure 11: Board thermal map (BIB10)

VIII. CONCLUSIONS

Using deep data extracted by the on-chip Agents while the DUTs are still under stress, the analytics running on the ELES ART platform add significant confidence for the efficiency of the stress conditions, improve reliability towards zero defects, shorten time to RCA, and lower cost to customers.

IX. REFERENCES

- [1] [STRESS-TEST-DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS | JEDEC](#)
- [2] IEEE IRPS 2019 | 15 Tutorial. Oliver, Aibel; Andreas, Aal
- [3] [Innovative reliability tests | Todi, PG | ELES S.p.A.](#)

