

RETE: Design and Test for Reliability

Data Analysis for Zero Defects

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Abstract— The challenges of modern automotive and mission critical applications require to go beyond the classical ways to perform IC Reliability Test and use innovative approaches to detect failures and measure performances degradation early in the development process, simplifying the search for their root causes and enabling an effective design and manufacturing process improvement for Zero Defects.

The application of accelerated stress and test together in the same equipment during qualification trials (TfR - Test for Reliability), leveraging on Reliability Test oriented IC testability (DfRT) and a DfT Adaptive Reliability Tester allows to set-up and guarantee the correct stress level in line with Mission Profile and continuously observe the evolution of the device behavior during the application of stress conditions.

This methodology – RETE (Reliability Embedding Test Engineering) is fully synergic with Silicon Lifecycle Management approach and provides at an early IC development stage, insights on device key reliability parameters and continuous degradation monitor with fine granularity, going beyond the approach based on standard checkpoints pre/post stress.

Embedding Test phases into the qualification flow enhance also failure detection capabilities (intermittent failure included) and observation of how IC signals have evolved leading to the appearance of the actual failure.

The analysis of all these data sets from qualification lots supported by Data Analytics Tools ease the process of identification of anomalous situations and how and why these anomalies presented themselves, eventually points us quickly in the direction of the causes of the failure, whether related to design or manufacturing process weaknesses.

With this approach it is possible to achieve the challenging quality and reliability targets required for automotive and mission critical applications, allowing a smooth and fast path towards zero-defects at a sustainable cost.

In this paper we describe the case of an HTOL qualification trial on a System on Chip device in an advanced technology node.

The High Operating Temperature Life test (HTOL) is the main trial to assess the intrinsic reliability of a solid-state device. It requires the application of high temperature and high voltage stress on the device, for a certain number of hours and sample size. During the HTOL, the device is stressed in dynamic configuration, trying to satisfy as much as possible the following conditions:

- o Application stress condition.
- o Maximum operative supply voltage and worst-case operative voltage.
- o Maximum current load
- o Maximum operative junction temperature.

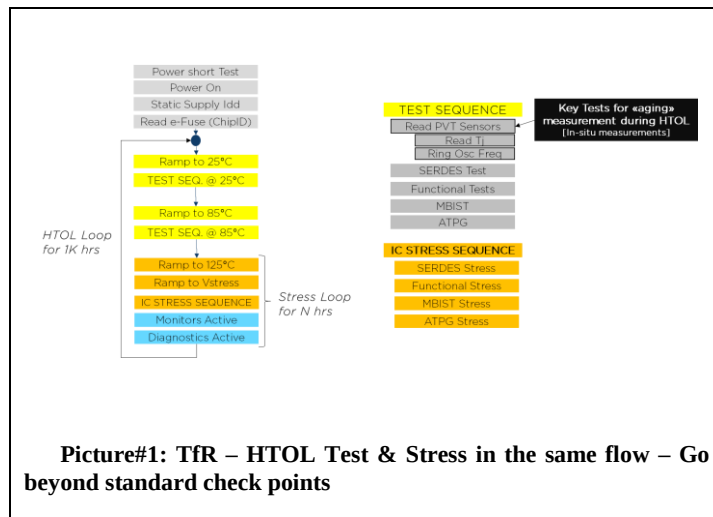
This test simulates and accelerates the application conditions. The goal is to cover the expected lifetime of the device in its application on the field, in the limited timeframe (typically 1000 hours) of the trial executed on a typical lot of 80 parts. The effect of the HTOL is the ageing of the device, to activate the dominant failure mechanism in the relatively short duration of the trial. In advanced node technologies it is becoming more and more important to have real time monitoring of the main parameters, not only to detect hard failures but also variations or drifts. At this purpose the IC was instrumented during design phase embedding 9 PVT sensors for real time T_j acquisition and in-situ aging measurement during reliability trials.

The HTOL flow, including all the in-situ measurements – has been performed applying a TfR flow approach where stress, test and monitoring are performed in a unique insertion on a DfT adaptive reliability tester – ART. This methodology allows a continuous degradation to monitor with fine granularity and the possibility also to capture and characterize possible stress driven failures detected during and post-stress.

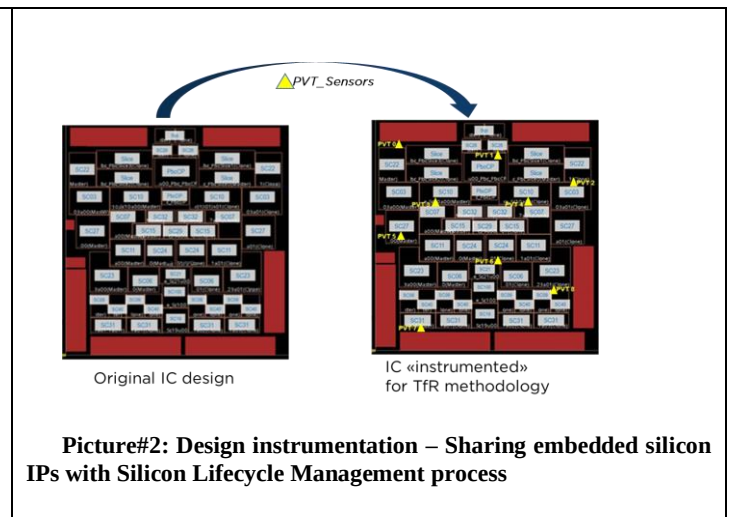
The value of the temperature of each embedded sensor (PVT) is read and logged in order to have detailed information about the internal junction temperature related to each test pattern (Hot Spot measurement). The target is to guarantee correct stress conditions alongside the chip area in line with Mission Profile, so real time T_j sense reading is fundamental.

At the end of each of the stress phases, the Process Sensor (PVT) output is acquired. The output of the Process Sensor is a proportional value to the frequency of ring oscillator, this last parameter is impacted (drift) by the application of the accelerated stress. Based on these readings, distributed along the HTOL experiments, different types of analysis are possible. The automatic and continuous performance degradation monitor on a wide sample basis and at different stress conditions allows to gather relevant information to better characterize aging phenomena during time and detect early possible outliers, information of outmost importance for

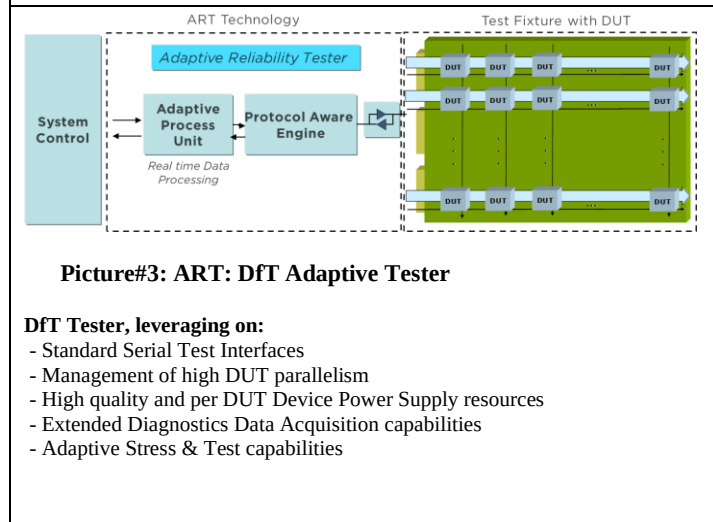
complete reliability assessment driving design and process improvement.



Picture#1: Tfr – HTOL Test & Stress in the same flow – Go beyond standard check points



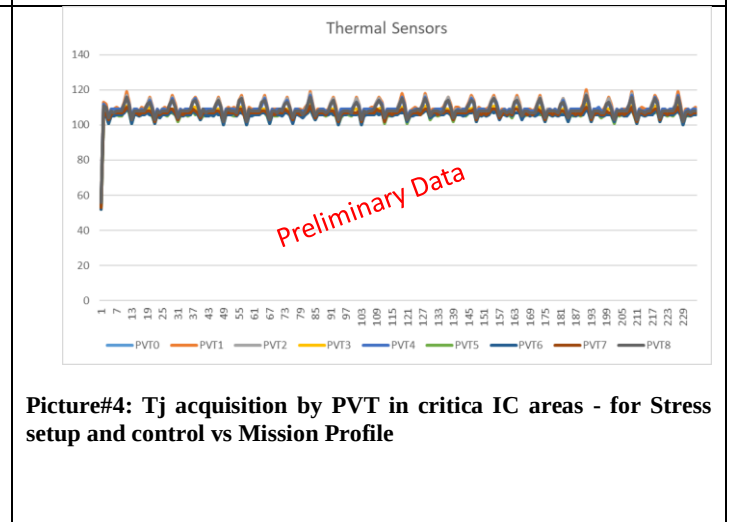
Picture#2: Design instrumentation – Sharing embedded silicon IPs with Silicon Lifecycle Management process



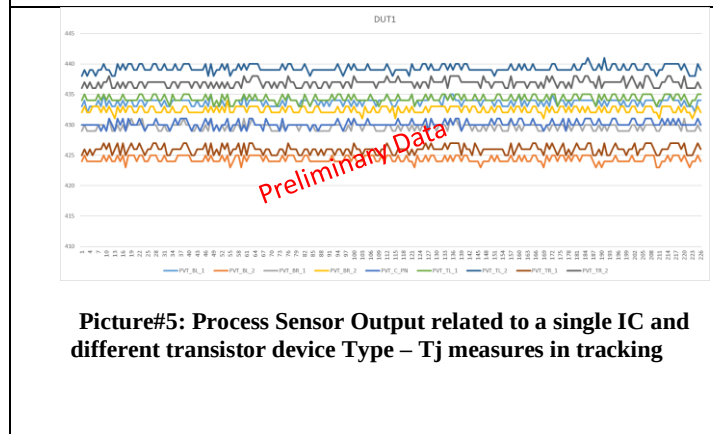
Picture#3: ART: Dft Adaptive Tester

Dft Tester, leveraging on:

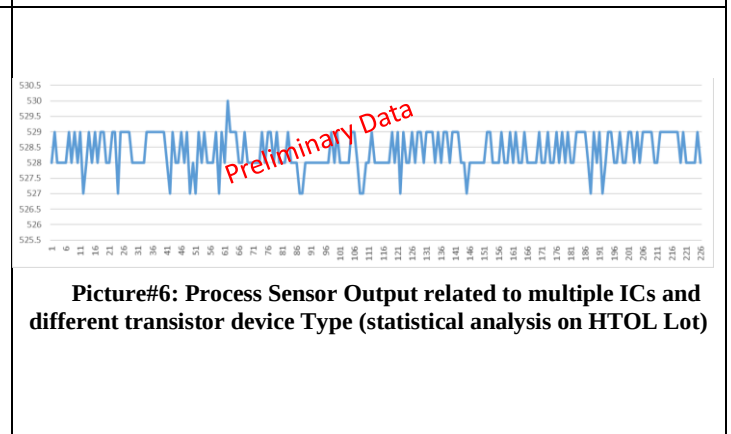
- Standard Serial Test Interfaces
- Management of high DUT parallelism
- High quality and per DUT Device Power Supply resources
- Extended Diagnostics Data Acquisition capabilities
- Adaptive Stress & Test capabilities



Picture#4: Tj acquisition by PVT in critica IC areas - for Stress setup and control vs Mission Profile



Picture#5: Process Sensor Output related to a single IC and different transistor device Type – Tj measures in tracking



Picture#6: Process Sensor Output related to multiple ICs and different transistor device Type (statistical analysis on HTOL Lot)